ANALOG CIRCUITS LAB

Third Semester – Electronics and Communication Engineering

College of Engineering Trivandrum

Laboratory Experiment Report

Experiment No.	05	**Date of Experiment**	_____
Experiment Title	Design and Setup of an RC-Coupled Common-Emitter Amplifier Using a BJT		
Student Name	_____	**Roll No.**	_____
University Reg. No.	_____	**Batch / Group**	_____
Team Member(s)	_____		
Course Instructor	_____	**Lab Instructor / TA**	_____
Time of Experiment	_____	**Laboratory / Workstation**	_____
Date of Submission	_____	**Student Signature**	_____

Engineering Challenge and Deliverables

Challenge statement: Design, simulate, construct, and evaluate a single-stage RC-coupled common-emitter BJT amplifier that operates in the active region and provides stable voltage amplification over a specified frequency range.

Example design requirements:

- DC supply: $V_{CC} = 12\,\text{V}$.
- Quiescent collector-emitter voltage near the middle of the available output-swing range.
- Midband voltage gain magnitude greater than $60\,\text{V/V}$.
- Lower cutoff frequency below $100\,\text{Hz}$.
- Undistorted sinusoidal output for the prescribed small input signal.

Required deliverables: completed pre-lab design, simulation, neat circuit schematic, verified instrument and component list, recorded raw measurements, calculations, frequency-response graph, theory–simulation–measurement comparison, uncertainty/error analysis, conclusion, and an individually written report.

Pre-lab requirement

The student should read the complete experiment, review the relevant theory, finish the required calculations and simulation, predict the expected waveforms, and prepare observation tables *before* entering the laboratory. The pre-lab is part of the engineering design process, not an optional preliminary exercise.

Laboratory safety and conduct

Switch off the DC supply before inserting, removing, or rewiring components. Set a suitable current limit before energising the circuit. Verify transistor pin configuration and electrolytic-capacitor polarity. Never measure resistance in an energised circuit. Use a common ground correctly, avoid shorting the supply through oscilloscope ground leads, and return instruments, components, and leads to their designated locations after the experiment.

1 Objective

What the student should include

- State the purpose in measurable engineering terms.
- Identify the circuit topology and the quantities to be designed, measured, and compared.
- Relate the objectives to the challenge specifications.
- Avoid vague wording such as "to study the amplifier."

Illustrative example: RC-coupled BJT amplifier

The objectives of the experiment are:

1. To design and construct a single-stage RC-coupled common-emitter amplifier using an NPN BJT.
2. To establish a stable DC operating point that permits approximately symmetrical output-voltage swing.
3. To simulate and experimentally determine the midband voltage gain, lower cutoff frequency, upper cutoff frequency, and bandwidth.
4. To observe the approximately 180° phase reversal between input and output.
5. To compare theoretical, simulated, and experimental values and explain the important differences using component tolerance, transistor variation, loading, and parasitic effects.

2 Background Theory

What the student should include

- Establish the scientific and engineering context of the experiment.
- Explain the operation of the common-emitter amplifier and the purpose of each resistor and capacitor.
- Present only the equations needed for design and interpretation.
- State assumptions, including active-region operation, small-signal excitation, room temperature, and nominal transistor current gain.
- Include a clear prediction or design hypothesis that will later be tested by the measurements.
- Cite the textbook, laboratory manual, datasheet, or other sources used.

Illustrative example: RC-coupled BJT amplifier

A common-emitter amplifier produces voltage gain and an output that is approximately 180° out of phase with its input. The voltage-divider network R_1–R_2 biases the transistor base. The emitter resistor R_E improves thermal and bias stability, while R_C converts changes in collector current into changes in collector voltage.
The coupling capacitors C_1 and C_2 pass the AC signal while isolating the DC bias of the amplifier from the source and load. The emitter-bypass capacitor C_E provides a low-reactance AC path around R_E in the intended frequency band, thereby increasing AC gain without removing DC stabilisation.
For a transistor operating in its active region,

$$I_C \approx \beta I_B, \tag{1}$$
$$I_E \approx (\beta + 1) I_B, \tag{2}$$
$$V_{CE} = V_C - V_E. \tag{3}$$

The intrinsic small-signal emitter resistance is approximately

$$r_e \approx \frac{V_T}{I_E}, \tag{4}$$

where $V_T \approx 25\,\text{mV}$ at room temperature. When R_E is effectively bypassed at midband, an approximate stage gain is

$$A_v \approx -\frac{R_C \parallel R_L}{r_e + X_{C_E,\text{effective}}}. \tag{5}$$

A more accurate prediction should also include source loading, finite transistor current gain, transistor output resistance, and the bias network.
The lower cutoff frequency is governed mainly by C_1, C_2, and C_E. The upper cutoff frequency is governed mainly by transistor junction capacitances, the Miller effect, wiring capacitance, and probe loading. The bandwidth is

$$BW = f_H - f_L. \tag{6}$$

Design hypothesis: If the transistor is biased near the middle of its usable output-swing range and the capacitors are selected so that their reactances are sufficiently small in the midband, the constructed circuit will provide a nearly constant midband gain greater than 60 V/V, with reduced gain below f_L and above f_H.

3 Circuit Diagram

What the student should include

- Draw a neat schematic showing correct interconnections.
- Label the transistor, all component reference names and values, V_{CC}, input, output, and ground.
- Mark important measurement nodes: base, collector, and emitter.
- Show the source resistance and external load when they affect results.
- Ensure the final schematic represents the circuit actually built; document any in-lab component substitution.

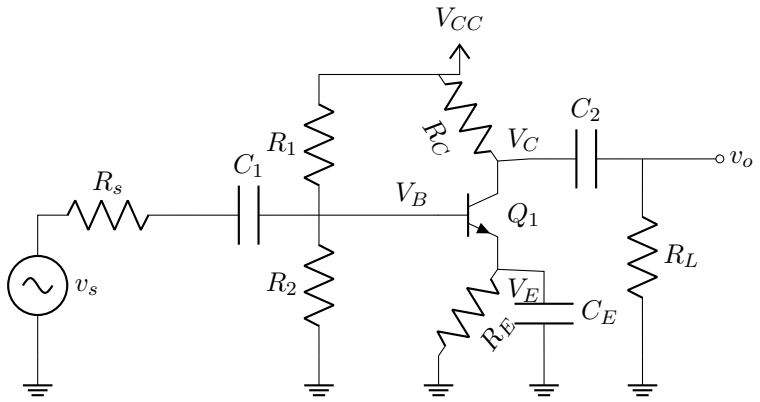

Figure 1: Single-stage RC-coupled common-emitter BJT amplifier.

Illustrative example: RC-coupled BJT amplifier

Item	Nominal value / type	Function
Q_1	BC547B	NPN amplifying device
V_{CC}	12 V	DC supply
R_1	100 kΩ	Upper bias resistor
R_2	18 kΩ	Lower bias resistor
R_C	4.7 kΩ	Collector resistor
R_E	1 kΩ	DC stabilisation resistor
C_1	1 µF	Input coupling capacitor
C_2	1 µF	Output coupling capacitor
C_E	47 µF	Emitter bypass capacitor
R_L	10 kΩ	External load
R_s	600 Ω	Representative source resistance

4 Equipment and Software Required

What the student should include

- Specify every test instrument using manufacturer and model/type number.
- Record relevant instrument settings or specifications such as bandwidth, input impedance, probe attenuation, and source impedance.
- List component type, nominal value, measured value, tolerance, and power or voltage rating where relevant.
- Identify the simulator, software version, transistor model/library, and analyses performed.
- List breadboard, probes, BNC leads, connecting wires, and other materials required for reproducibility.

Illustrative example: RC-coupled BJT amplifier

Illustrative equipment list:

- Regulated DC power supply, 0 V to 30 V, with current-limit facility; manufacturer/model: _____.
- Dual-channel digital storage oscilloscope, minimum 20 MHz bandwidth; manufacturer/model: _____.
- Function generator with sine-wave output; manufacturer/model: _____.
- Digital multimeter; manufacturer/model: _____.
- Two 10× oscilloscope probes, breadboard, BNC leads, and connecting wires.
- BC547B NPN transistor, resistors, and capacitors listed with Figure 1.
- LTspice / PSpice / Multisim, version: _____; transistor model: _____.

Component-verification table:

Component	Nominal	Measured	Tolerance/rating	Used value
R_1	100 kΩ	98.7 kΩ	±5%	98.7 kΩ
R_2	18 kΩ	17.9 kΩ	±5%	17.9 kΩ
R_C	4.7 kΩ	4.66 kΩ	±5%	4.66 kΩ
R_E	1 kΩ	0.99 kΩ	±5%	0.99 kΩ
C_E	47 µF	—	25 V, ±20%	47 µF

5 Pre-Lab Calculations and Design

What the student should include

- Record initial thoughts on how the challenge can be solved.
- State design specifications, assumptions, and the proposed topology.
- Complete DC bias design, small-signal analysis, capacitor selection, predicted gain, output swing, and cutoff-frequency calculations.
- Use standard component values and then recompute expected performance.
- Prepare expected waveforms and an expected frequency-response sketch.
- Perform and document DC operating-point, AC sweep, and transient simulations before construction.
- Identify risks and checks: transistor pinout, clipping, saturation, capacitor polarity, and maximum device ratings.

6.1 Initial thoughts and proposed solution

Illustrative example: RC-coupled BJT amplifier

A voltage-divider-biased common-emitter stage was selected because it provides higher bias stability than fixed bias. An emitter resistor was retained for DC negative feedback, while a bypass capacitor was added to obtain higher AC gain. The collector voltage was targeted near the middle of the supply range to allow approximately symmetrical output swing. Input and output coupling capacitors were used to prevent the source and load from disturbing the DC bias.
The design was expected to meet the gain requirement if the transistor remained in the active region and the emitter bypass capacitor presented sufficiently low reactance in the intended midband.

6.2 DC bias design

Illustrative example: RC-coupled BJT amplifier

Assume

$$V_{CC} = 12\,\mathrm{V}, \qquad \beta = 100, \qquad V_{BE} = 0.7\,\mathrm{V}, \qquad R_E = 1\,\mathrm{k\Omega}.$$

For $R_1 = 100\,\mathrm{k\Omega}$ and $R_2 = 18\,\mathrm{k\Omega}$, the Thevenin equivalent at the base is

$$V_{TH} = V_{CC}\frac{R_2}{R_1 + R_2} = 12\frac{18}{100 + 18} = 1.83\,\mathrm{V}, \tag{7}$$

$$R_{TH} = R_1 \parallel R_2 = 15.25\,\mathrm{k\Omega}. \tag{8}$$

The base current is estimated as

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E} = \frac{1.83 - 0.70}{15.25\,\mathrm{k} + 101(1\,\mathrm{k})} \approx 9.72\,\mu\mathrm{A}. \tag{9}$$

Therefore,

$$I_C \approx \beta I_B = 0.972\,\mathrm{mA}, \tag{10}$$

$$I_E \approx (\beta + 1)I_B = 0.982\,\mathrm{mA}, \tag{11}$$

$$V_E = I_E R_E \approx 0.982\,\mathrm{V}, \tag{12}$$

$$V_C = V_{CC} - I_C R_C \approx 12 - (0.972\,\mathrm{m})(4.7\,\mathrm{k}) = 7.43\,\mathrm{V}, \tag{13}$$

$$V_{CE} = V_C - V_E \approx 6.45\,\mathrm{V}. \tag{14}$$

Since V_{CE} is well above saturation voltage and below the supply voltage, the predicted operating point lies in the active region.

6.3 Small-signal and capacitor design

Illustrative example: RC-coupled BJT amplifier

The intrinsic emitter resistance is

$$r_e \approx \frac{25\,\text{mV}}{0.982\,\text{mA}} \approx 25.5\,\Omega. \tag{15}$$

The effective AC collector load is

$$R_C \parallel R_L = 4.7\,\text{k}\Omega \parallel 10\,\text{k}\Omega \approx 3.20\,\text{k}\Omega. \tag{16}$$

Ignoring loading and nonidealities, the upper-bound midband gain magnitude is approximately

$$|A_v| \approx \frac{R_C \parallel R_L}{r_e} \approx \frac{3.20\,\text{k}}{25.5} \approx 125\,\text{V/V}. \tag{17}$$

The practical overall gain is expected to be lower because of source loading, finite bypass-capacitor impedance, finite β, and transistor output resistance.
For a coupling capacitor with an approximate resistance of $2.8\,\text{k}\Omega$ and a target pole below $100\,\text{Hz}$,

$$C_1 \geq \frac{1}{2\pi f R} = \frac{1}{2\pi(100)(2.8\times10^3)} \approx 0.57\,\mu\text{F}. \tag{18}$$

The next convenient standard value, $C_1 = 1\,\mu\text{F}$, was selected. Similarly, $C_2 = 1\,\mu\text{F}$ and $C_E = 47\,\mu\text{F}$ were selected.
At $1\,\text{kHz}$,

$$|X_{C_E}| = \frac{1}{2\pi f C_E} = \frac{1}{2\pi(1000)(47\times10^{-6})} \approx 3.39\,\Omega, \tag{19}$$

which is much smaller than R_E, supporting the bypass approximation at midband.

6.4 Pre-lab simulation plan and prediction

Illustrative example: RC-coupled BJT amplifier

The following simulations should be completed before the laboratory:

1. **DC operating point:** record V_B, V_E, V_C, V_{CE}, and transistor currents.
2. **AC sweep:** use a logarithmic sweep covering at least $10\,\text{Hz}$ to $1\,\text{MHz}$; estimate midband gain, f_L, f_H, and bandwidth.
3. **Transient analysis:** apply the prescribed small sinusoidal input and verify output amplitude, phase inversion, and absence of clipping.
4. **Optional robustness checks:** vary transistor β, resistor tolerance, capacitor tolerance, and temperature.

An illustrative simulation predicted a midband gain of approximately $76\,\text{V/V}$, a lower cutoff frequency of $74\,\text{Hz}$, and an upper cutoff frequency of $260\,\text{kHz}$.

Instructor verification

Pre-lab completed: Yes / No Instructor initials and date: _____

6 Experimental Setup

What the student should include

- Describe in paragraph form what was actually done, not merely what the manual instructed.
- Use past tense for completed experimental actions.
- Include enough detail for another student to reproduce the work.
- State supply current limit, signal amplitude, waveform, frequency, offset, source impedance, oscilloscope coupling, termination, probe setting, and measurement points.
- Describe the order of DC checks, AC tests, and frequency sweep.
- Record any deviation, troubleshooting step, or component replacement.
- Do not insert measured results in the procedure description.

Illustrative example: RC-coupled BJT amplifier

The resistor values were first verified using a digital multimeter, and the BC547B pin configuration was checked from its datasheet. The circuit in Figure 1 was assembled on a solderless breadboard with short interconnections and a common ground rail. Electrolytic-capacitor polarity was verified before power was applied.

The DC supply was initially switched off, set to 12 V, and given a current limit of 50 mA. After a visual continuity and wiring check, the supply was switched on. The base, emitter, and collector DC voltages were measured before applying any signal. The supply was switched off before any correction to the circuit.

A zero-offset sinusoidal signal of 20 mV RMS was then applied through C_1. Oscilloscope Channel 1 measured the amplifier input and Channel 2 measured the output across R_L. Both probes were set to 10× attenuation and were compensated before use.

For the frequency-response test, the input amplitude was kept approximately constant while frequency was varied logarithmically from 10 Hz to 500 kHz. At every frequency, the actual input and output amplitudes were recorded. Measurements near the cutoff frequencies were repeated with finer frequency increments. The phase relation and onset of clipping were observed separately at 1 kHz.

7.1 Experimental setup record

Supply setting and current limit _____

Input waveform, amplitude, offset _____

Source output/termination setting _____

Oscilloscope probe and coupling _____

Load connected _____

Circuit changes from pre-lab design _____

7 Data and Observations

What the student should include

- Record measurements during the experiment in a bound laboratory notebook or approved record.
- Present neat tables showing variable names, values, and units.
- Distinguish theoretical, simulated, and measured values.
- Retain the actual measured input at every frequency; do not assume the generator setting equals the circuit input.
- Record qualitative observations such as phase inversion, clipping, noise, oscillation, drift, or waveform distortion.
- Re-measure anomalous data or verify it using a different measurement method; document the check instead of silently deleting the point.
- Obtain instructor verification of the recorded raw data when required.

8.1 DC operating-point observations

Quantity	Theory	Simulation	Measurement	Measurement–theory error
V_B	1.68 V	1.67 V	1.66 V	−1.2%
V_E	0.98 V	0.97 V	0.96 V	−2.0%
V_C	7.43 V	7.37 V	7.31 V	−1.6%
V_{CE}	6.45 V	6.40 V	6.35 V	−1.6%

8.2 Frequency-response observations

Table 1: Illustrative frequency-response observations.

Frequency	V_{in}	V_{out}	$\lvert A_v\rvert = V_{out}/V_{in}$	Gain (dB)
10 Hz	20 mV	0.100 V	5.00	13.98
20 Hz	20 mV	0.240 V	12.0	21.58
50 Hz	20 mV	0.700 V	35.0	30.88
80 Hz	20 mV	1.010 V	50.5	34.07
100 Hz	20 mV	1.120 V	56.0	34.96
200 Hz	20 mV	1.360 V	68.0	36.65
500 Hz	20 mV	1.424 V	71.2	37.05
1 kHz	20 mV	1.430 V	71.5	37.09
5 kHz	20 mV	1.428 V	71.4	37.08
10 kHz	20 mV	1.424 V	71.2	37.05
50 kHz	20 mV	1.380 V	69.0	36.78
100 kHz	20 mV	1.280 V	64.0	36.12
200 kHz	20 mV	1.060 V	53.0	34.49
240 kHz	20 mV	1.010 V	50.5	34.07
300 kHz	20 mV	0.880 V	44.0	32.87
500 kHz	20 mV	0.580 V	29.0	29.25

8.3 Qualitative observations and anomaly log

Illustrative example: RC-coupled BJT amplifier

At 1 kHz, the output was sinusoidal and approximately 180° out of phase with the input. Visible clipping appeared when the input was increased beyond approximately 65 mV RMS. No sustained oscillation was observed.
The first reading near 200 kHz was inconsistent with adjacent measurements. The probe compensation and generator amplitude were checked, and the measurement was repeated. The repeated value was used and the original reading was retained in the laboratory notebook.

Condition	Observation or anomaly	Recheck/corrective action

Instructor verification

Raw data checked during/after the experiment:

Instructor / TA name: _____ Signature and date: _____

8 Sample Calculations

What the student should include

- Show one complete worked example for every type of calculation.
- Substitute numerical values with units before stating the result.
- Include voltage gain, gain in decibels, −3 dB level, cutoff frequencies, bandwidth, and percentage error.
- State how graph-derived quantities were obtained.
- Use suitable significant figures consistent with instrument resolution and uncertainty.

Illustrative example: RC-coupled BJT amplifier

At 1 kHz,

$$|A_v| = \frac{V_{out}}{V_{in}} = \frac{1.430\,\text{V}}{20\,\text{mV}} = 71.5\,\text{V/V}, \tag{20}$$

$$A_v(\text{dB}) = 20\log_{10}(71.5) = 37.09\,\text{dB}. \tag{21}$$

The -3 dB level is

$$A_{-3\,\text{dB}} = 37.09 - 3 = 34.09\,\text{dB}. \tag{22}$$

From the graph,

$$f_L \approx 80\,\text{Hz}, \qquad f_H \approx 240\,\text{kHz}.$$

Hence,

$$BW = f_H - f_L = 240000 - 80 = 239.92\,\text{kHz}. \tag{23}$$

The percentage error in the measured midband gain relative to the simulated gain is

$$\%\,\text{error} = \frac{|A_{v,\text{meas}} - A_{v,\text{sim}}|}{A_{v,\text{sim}}} \times 100 = \frac{|71.5 - 76|}{76} \times 100 = 5.9\%. \tag{24}$$

The percentage error in the measured collector-emitter voltage relative to the theoretical value is

$$\%\,\text{error} = \frac{|6.35 - 6.45|}{6.45} \times 100 = 1.55\%. \tag{25}$$

9 Graphs

What the student should include

- Give every graph a specific title and figure number.
- Label both axes with variable names and correct units.
- Plot every measured data point; do not draw an unsupported smooth curve through omitted points.
- Use logarithmic frequency scale for amplifier frequency response.
- Distinguish measured, theoretical, and simulated curves using a legend.
- Mark the midband gain, -3 dB level, f_L, and f_H.
- Explain in the text how the important parameters were obtained.
- Use exported publication-quality plots rather than screenshots that contain menus or unreadable cursor text.

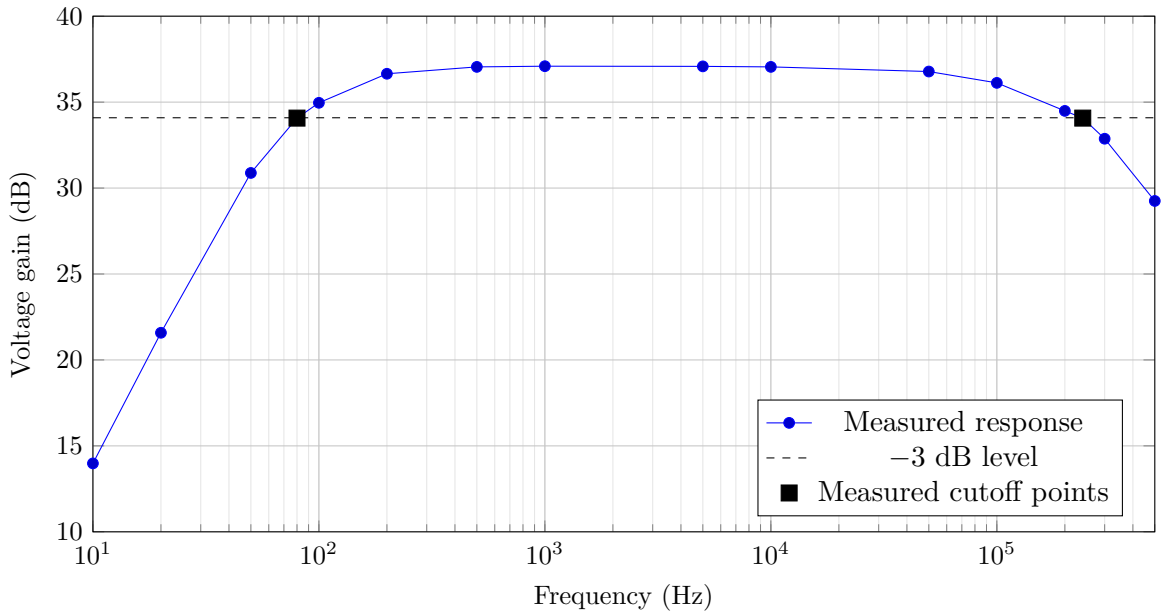

Figure 2: Illustrative measured frequency response of the RC-coupled amplifier.

Illustrative example: RC-coupled BJT amplifier

Figure 2 shows an approximately constant gain in the midband. The low-frequency reduction is caused by the finite reactances of C_1, C_2, and C_E. The high-frequency reduction is associated with transistor junction capacitances, the Miller effect, breadboard parasitic capacitance, and oscilloscope-probe loading. The measured -3 dB intersections occur near 80 Hz and 240 kHz.

10 Results and Discussion

What the student should include

- Begin with a concise summary of the principal findings.
- State whether the measurements support the design hypothesis and whether every specification was met.
- Compare theoretical, simulated, and measured values quantitatively.
- Refer directly to tables and figures as evidence.
- Explain discrepancies using component tolerance, transistor spread, source/load effects, probe capacitance, breadboard parasitics, noise, temperature, model limitations, and instrument uncertainty.
- Do not call every discrepancy "human error." Give a testable circuit-level explanation.
- Do not introduce new results that were not presented in the Data, Observations, or Graphs sections.
- Discuss troubleshooting, repeatability, limitations, and technically justified improvements.

Parameter	Theory	Simulation	Measurement	Error	Interpretation
V_{CE}	6.45 V	6.40 V	6.35 V	1.55%	Active-region bias achieved
Midband gain	84 V/V	76 V/V	71.5 V/V	5.9% vs. simulation	Gain requirement satisfied
f_L	70 Hz	74 Hz	80 Hz	8.1% vs. simulation	Capacitor tolerance and combined poles
f_H	—	260 kHz	240 kHz	7.7% vs. simulation	Parasitic and probe capacitance
Bandwidth	—	259.93 kHz	239.92 kHz	7.7% vs. simulation	Broadband response obtained

Illustrative example: RC-coupled BJT amplifier

The measured DC operating point was $V_{CE} = 6.35\,\text{V}$, close to the theoretical 6.45 V. This confirms that the transistor operated in the active region and that the voltage-divider bias provided an appropriate quiescent point.
The measured midband gain was 71.5 V/V, compared with the simulated 76 V/V. The measured value exceeded the stated requirement of 60 V/V, so the gain specification was met. The remaining difference is consistent with transistor-β variation, finite output resistance, nonzero emitter-bypass reactance, loading by the source and oscilloscope, and resistor tolerance.
The measured lower cutoff frequency was approximately 80 Hz, slightly above the simulated 74 Hz. Electrolytic capacitors commonly have wider tolerance than resistors, and the observed low-frequency response is the combined effect of multiple poles rather than a single ideal pole.
The measured upper cutoff frequency was approximately 240 kHz, below the simulated 260 kHz. The likely causes are transistor junction-capacitance variation, the Miller effect, breadboard wiring capacitance, and probe capacitance that may not have been fully represented in the simulation.
The output phase reversal agreed with common-emitter theory. The small-signal output remained approximately sinusoidal, while larger inputs caused clipping as the transistor approached cutoff or saturation. Thus, the experimental observations supported the design hypothesis within the limitations of the components, model, and measurement setup.
A more rigorous follow-up could repeat the test using several transistor samples, measure actual capacitor values, include probe capacitance in the simulation, and construct the circuit on a PCB with shorter interconnections.

11.1 Measurement uncertainty and limitations

Illustrative example: RC-coupled BJT amplifier

The reported results should be interpreted with the following limitations:

- resistor and capacitor tolerance;
- unit-to-unit variation in BJT β, V_{BE}, and junction capacitances;
- oscilloscope amplitude accuracy, bandwidth, and probe capacitance;
- function-generator source resistance and frequency-dependent output;
- breadboard contact resistance and stray capacitance;
- finite reading resolution and possible temperature drift;
- differences between the simulator device model and the physical transistor.

Where a discrepancy changes the conclusion, estimate its uncertainty or repeat the measurement rather than merely listing possible error sources.

11 Conclusions

What the student should include

- Directly answer the objectives and the engineering challenge.
- State the most important measured numerical results.
- Clearly identify which specifications were or were not achieved.
- State what was learned about the circuit, design process, simulation, measurement, and evidence-based engineering judgment.
- Mention only improvements supported by the preceding analysis.
- Do not introduce new data or lengthy theory.

Illustrative example: RC-coupled BJT amplifier

A voltage-divider-biased, single-stage RC-coupled common-emitter amplifier was designed, simulated, constructed, and tested. The measured quiescent collector-emitter voltage was 6.35 V, confirming active-region operation. The measured midband gain was approximately 71.5 V/V, and the output was approximately 180° out of phase with the input. The lower and upper cutoff frequencies were approximately 80 Hz and 240 kHz, giving a bandwidth of approximately 239.92 kHz.

The gain and lower-cutoff specifications were achieved. The measured results were reasonably close to simulation, and the differences were consistent with component tolerance, transistor parameter variation, loading, and breadboard/probe parasitics. The experiment demonstrated the complete engineering cycle of defining a problem, carrying out pre-lab design and simulation, constructing and testing the circuit, analysing evidence, explaining discrepancies, and communicating the outcome in a formal report.

12 References

What the student should include

- List every source actually used: laboratory manual, textbooks, datasheets, simulator documentation, standards, and technical notes.
- Use a consistent engineering citation style, preferably IEEE style.
- Cite a source in the body wherever its equation, model, specification, figure, or design rule is used.
- Do not list sources that were not consulted.

References

[1] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 8th ed. New York, NY, USA: Oxford University Press, 2020.

[2] R. L. Boylestad and L. Nashelsky, *Electronic Devices and Circuit Theory*, 11th ed. Boston, MA, USA: Pearson, 2013.

[3] onsemi, "BC546B, BC547A/B/C, BC548B/C NPN General-Purpose Transistors," BC547 series datasheet.

[4] Analog Devices, "LTspice Simulator Documentation," software documentation, accessed August 4, 2026.

[5] Department of Electronics and Communication Engineering, *Analog Circuits Laboratory Manual*, College of Engineering Trivandrum, current academic year.

[6] Muthoot Institute of Technology and Science, *Electronics Circuits Lab Manual*, laboratory instruction and technical-report guidance.

A Optional Appendix: Raw Data, Simulation, and Supporting Material

Use appendices for material that supports verification but would interrupt the main report:

- complete unprocessed measurements and repeated trials;
- oscilloscope captures with scale, coupling, and probe information;
- SPICE netlist, model statement, and simulation settings;
- additional theoretical derivations;
- uncertainty calculations;
- measured component values and calibration information;
- photographs used to clarify breadboard layout or troubleshooting.

The main report should remain understandable without requiring the reader to search through the appendices.

B Student Authorship and Team-Contribution Declaration

Laboratory construction and data collection may be carried out as a team when permitted by the instructor. However, the interpretation and written report submitted under a student's name should be that student's own work, except for properly acknowledged collaboration and cited sources.

Student's contribution	_____
Team members' contribution	_____
Shared data or resources used	_____
Student declaration	I confirm that this report accurately records the work performed and that the submitted analysis and writing comply with the course instructions.
Student signature and date	_____

C Instructor Evaluation

This section is to be completed by the instructor or laboratory evaluator. The assessment records preparation, experimental competence, understanding, and continuous maintenance of the laboratory report/record.

Sl. No.	Evaluation Component and Indicators	Maximum Marks	Marks Awarded
1	**Preparation / Pre-Lab Work** • familiarity with the objective, theory, circuit, and procedure; • completed design calculations and expected waveforms; • completed simulation and prepared observation tables; • component, pinout, rating, and safety checks.	**14**	
2	**In-Lab Experimental Performance** • systematic circuit assembly and correct instrument connections; • safe operation and proper use of power supply, DMM, function generator, and oscilloscope; • accurate measurement and recording of data; • logical troubleshooting and rechecking of anomalous readings; • teamwork, care of equipment, and orderly completion of the experiment.	**14**	
3	**Viva Voce** • understanding of circuit operation and design choices; • ability to explain expected and measured waveforms; • interpretation of gain, cutoff frequencies, bandwidth, biasing, loading, and sources of discrepancy.	**20**	
4	**Timely Completion of Lab Reports / Record (Continuous Assessment)** • regular and timely completion; • complete observations, calculations, graphs, and results; • comparison of theory, simulation, and experiment; • clarity, organisation, technical accuracy, and neatness.	**12**	
	Total	**60**	

Instructor's remarks _____

_____

Performance grade _____

Date _____

Instructor's name and signature _____