10	Transistor series voltage regulator – Design for a specific output voltage with & without short circuit protection (plot load & line regulation characteristics).
Part B – Simulation Experiments (Any *Six* experiments mandatory) The experiments shall be conducted using Open-Source Tools such as QUCS, KiCad, LT SPICE, or variants of SPICE tools.	
1	RC Integrating and Differentiating Circuits – (Transient analysis with different inputs and frequency response)
2	Diode Clipping and Clamping Circuits (Transient and transfer characteristics)
3	CE amplifier – Design for a specific voltage gain and plot frequency response characteristics
4	CS MOSFET amplifier - Design for a specific voltage gain and plot frequency response characteristics
5	Cascaded amplifier (CE – CE) - Design for a specific voltage gain and plot frequency response characteristics
6	Cascode amplifier - Design for a specific voltage gain and plot frequency response characteristics
7	Feedback amplifiers (current series & voltage series) - Design for a specific voltage gain and plot frequency response characteristics
8	RC oscillators – RC phase shift or wien bridge oscillator
9	Power amplifiers (Transformer less) – Class B & Class AB
10	Transistor series voltage regulator – Design for a specific output voltage with & without short circuit protection (plot load & line regulation characteristics).

Course Assessment Method
(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)	Internal Examination	Total
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

- ***Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.***
- ***Endorsement by External Examiner:*** *The external examiner shall endorse the record*

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design and demonstrate the functioning of basic analog circuits using discrete components.	**K3**
CO2	Design and simulate the functioning of basic analog circuits using simulation tools	**K3**
CO3	Conduct troubleshooting of a given circuit and to analyze it	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO- PO Mapping (Mapping of Course Outcomes with Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2						3			3
CO2	3	2	2		3				3			3
CO3	3	2	2						3			3

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Electronic Devices and Circuits	David A Bell	Oxford University Press, 2008	5th edition
2	Electronic Circuits Analysis and Design 1	D. Meganathan	Yes Dee Publishing, 2023	1st edition

Continuous Assessment (25 Marks)

1. **Preparation and Pre-Lab Work (7 Marks)**

   - Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
   - Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. **Conduct of Experiments (7 Marks)**

   - Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
   - Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
   - Teamwork: Collaboration and participation in group experiments.

3. **Lab Reports and Record Keeping (6 Marks)**

   - Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
   - Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**

   - Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**

    - Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
    - Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
    - Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
    - Creativity and logic in algorithm or experimental design.

2. **Conduct of Experiment/Execution of Work/Programming (15 Marks)**

    - Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and Result with Valid Inference/Quality of Output (10 Marks)

- Accuracy of Results: Precision and correctness of the obtained results.
- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

3. **Viva Voce (10 Marks)**

    - Ability to explain the experiment, procedure results and answer related questions
    - Proficiency in answering questions related to theoretical and practical aspects of the subject.

4. **Record (5 Marks)**

    - Completeness, clarity, and accuracy of the lab record submitted

SEMESTER S3
LOGIC CIRCUIT DESIGN LABORATORY

Course Code	**PCECL308**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Lab

Course Objectives:

1. Familiarise the students with the Digital Logic Design through the implementation of Logic Circuits.
2. Familiarise the students with the HDL based Digital Design and FPGA boards

Expt. No.	Experiments
Part A – List of Experiments using digital components (Any *Six* experiments mandatory)	
1	Realization of functions using basic and universal gates (SOP and POS forms).
2	Design and Realization of half/full adder and subtractor using basic gates and universal gates.
3	4 bit adder/subtractor and BCD adder using 7483
4	Study of Flip Flops : S-R, D, T, JK and Master slave JK FF using NAND gates
5	Asynchronous Counter : 3 bit up/down counter, Realization of Mod N Counter
6	Synchronous Counter: Realization of 4-bit up/down counter, Realization of Mod-N counters
7	Ring counter and Johnson Counter.
8	Realization of counters using IC's (7490, 7492, 7493).
9	Realization of combinational circuits using MUX & DEMUX, using ICs (74150, 74154)
10	Sequence Generator / Detector
Part B – Simulation Experiments (Any *Six* experiments mandatory) The experiments shall be conducted using Verilog and implementation using small FPGA	
1	Experiment 1: Realization of Logic Gates and Familiarization of FPGAs