PCECT303 ANALOG CIRCUITS • ANALOG CIRCUITS LABORATORY

COURSE PROJECT — STUDENT HANDBOOK

Semester S3 • B.Tech Electronics & Communication Engineering

Academic Year 2026–27 • Issued 06 August 2026 • Final submission 30 October 2026

Item	Detail
Component	Assignment / Micro-project component of Analog Circuits CIE — 15 marks
Team size	3 students per team (4 only with prior approval)
Mode	Hardware, simulation, or both — you choose. See Section 3. All three routes are marked on the same scale.
Budget ceiling	₹600 per team for components. Most projects cost far less. Nothing in this handbook requires you to buy an instrument.
Abstract due	Saturday, 15 August 2026 (11:59 PM)
Progress presentation	Week of 14–19 September 2026
Final presentation + demo + viva	27–29 October 2026
Final submission deadline	Friday, 30 October 2026 (11:59 PM)
Mapped COs	Theory CO1–CO4 (topic-dependent); Lab CO1, CO2, CO3 — all at K3

Read this first — the one thing that matters

This project is graded on **what you understand and how hard you worked**, not on whether your circuit finally worked. A team whose amplifier oscillates for three weeks, who chase it down methodically, document what they tried, and can explain in the viva why a long breadboard wire caused it, will score **higher** than a team whose circuit worked first time and who cannot say why they chose their emitter resistor.

In analog circuits, the gap between what you calculated, what the simulator predicted and what the multimeter reads is not an embarrassment. **It is the subject.** Your job is to measure that gap and explain it.

1. Purpose of the Project

In the lectures you analyse circuits that someone else designed. In the lab you follow a procedure that someone else wrote. This project is the first time you are asked to do the whole loop yourself: decide a specification, design a circuit to meet it, predict its behaviour, build or simulate it, measure what it actually does, and account for the difference.

> **This is not a lab experiment, and it should not look like one**
>
> Your lab sheet already asks you to design a CE amplifier for a specified gain and plot its frequency response. Doing that again, more carefully, is not a project. The answer is known before you start, the method is handed to you, and nothing about it can surprise you.
>
> A course project **starts** from the circuits in the syllabus and **goes past** them. It takes a familiar circuit and asks a question you have not been given the answer to — one that requires you to read a little beyond the course, measure something the lab sheet never asked for, or build something the syllabus assembles only in pieces.
>
> **The circuit may be familiar. The question must not be.** Every topic in Section 14 is chosen on that basis, and any topic you propose will be judged by it.

By the end you should be able to:

- Take a specification — "a voltage gain of 40, with the lower cut-off below 100 Hz, from a 12 V supply" — and produce a complete component list with every value justified by a calculation you can show.
- Predict a circuit's DC operating point and small-signal behaviour **before** switching it on, and be roughly right.
- Set up a SPICE simulation that answers a specific question, rather than one that produces a picture.
- Measure a real circuit correctly — knowing what your instrument can and cannot tell you.
- Explain a discrepancy quantitatively. "The measured gain was 34 instead of 40 because the transistor's actual β was 210, not the 300 I assumed, which raised r_e by …" is the sentence this project exists to teach you to write.
- Troubleshoot systematically instead of by swapping parts at random.

2. How This Project Is Graded

Assessment is weighted towards process and comprehension. Four mechanisms enforce this.

2.1 The three-way comparison

This is the technical core of every project in this course, whatever topic you choose. For each quantity that matters, you report **three numbers**:

Number	Where it comes from	Example
Designed	Your hand calculation, done before anything was built or simulated	$A_v = -g_m(R\_C \parallel R\_L) = -41.2$
Simulated	SPICE, with the model you chose and stated	−38.6 at 1 kHz

Number	Where it comes from	Example
Measured	The bench, with the instrument and settings stated	−34.1 ± 1.5 at 1 kHz

Then you explain the two gaps. Not "due to practical errors" — that phrase earns zero marks and we will ask you to replace it. A real explanation names the mechanism and, where possible, puts a number on it: the transistor's actual β measured on the DMM, the 5% resistor tolerance, the loading of the next stage, the meter's input impedance, the SPICE model's Early voltage.

Simulation-only teams substitute the third column with a *tolerance study*: a Monte-Carlo or worst-case corner run over 5% resistors, 20% electrolytics and β from 100 to 400. See Section 3.

2.2 The individual viva

At the final demonstration each member is questioned separately on any part of the project, including parts they did not personally do. Pointing at your teammate is not an answer. Divide the labour; do not divide the understanding.

2.3 The logbook

Each team keeps a **bound or stapled physical logbook** — a rough record — with one dated entry per working session. Photographs, waveform sketches, DMM readings, crossings-out and all. A sample entry:

```
12 Sep 2026   Anjali, Rahul, Fatima      4:30 - 6:15 pm
Built stage 1 on breadboard. Expected VE = 1.2 V, measured 0.31 V.
Checked: divider resistors correct (10k/2.2k measured 9.87k/2.19k).
VB measured 0.34 V -- far below the 1.9 V the divider should give.
Suspected transistor pinout. BC547 is C-B-E from flat face, we had
wired it as E-B-C. Reversed it -> VE = 1.18 V. Matches design.
Lesson: check pinout against datasheet, not against memory.
Next: bypass cap, then measure gain at 1 kHz.
```

The logbook is graded on **specificity and honesty, not on success**. Entries recording failures, wrong assumptions and dead ends are worth more than "worked on circuit". A logbook whose entries all date from the last week of October is a strong signal and will be read as one. Bring it to every review.

2.4 Analysis outweighs results

The marks for explaining your results exceed the marks for the results themselves. A circuit that misses its specification by 30%, with a correct explanation of why, scores above a circuit that hits it by luck.

This scores well	This scores poorly
A modest circuit where every component value traces back to a calculation	An elaborate circuit copied from a website with unexplained values
"Measured gain 34 vs designed 41; here is the β measurement that accounts for most of it"	"Gain was obtained as 34" with no comparison and no comment
Simulated and measured curves plotted on the same axes	Two separate plots on different scales in different sections
A logbook full of failed attempts	A logbook written the night before

This scores well	This scores poorly
"We never got it to stop oscillating. Here are the five things we tried and what each did."	Silence about the part that did not work

3. Choosing Your Mode: Hardware, Simulation, or Both

All three routes are available and all three are marked on the same 15-mark scale. What changes is what you must deliver to prove you understood the circuit.

Route	What it involves	Extra requirement, so that all routes are equally demanding
Hardware + simulation (recommended)	Design on paper, verify in SPICE, build on breadboard, measure, compare all three.	The full three-way comparison of Section 2.1, plus at least one documented troubleshooting episode.
Simulation only	Design on paper, then a thorough SPICE study — no physical build.	A tolerance and sensitivity study: Monte-Carlo over 5% resistors / 20% electrolytics / β = 100…400, plus a temperature sweep from 0 °C to 60 °C, plus a stated comparison against datasheet-typical behaviour. Depth substitutes for the bench.
Hardware only	Design and build, no simulator.	Not permitted as a whole project. You must simulate at least the DC operating point before powering anything, and you must include it in the report. This rule exists to save your components.

Which should you pick? If your team has any access to lab time and a multimeter, take the hardware route — the discrepancies you find are what make the project interesting, and the troubleshooting is where the learning is densest. Take the simulation-only route if scheduling is genuinely impossible, if your topic involves voltages or powers we would rather you did not handle in second year, or if your topic is one where the interesting behaviour is at frequencies you cannot measure with available instruments (crystal oscillators, class D switching).

> **A note on the honest middle path**
>
> Many good projects are **mostly** simulation with a partial build: the DC bias stage breadboarded and measured, the rest simulated. That is perfectly acceptable. Say clearly in the report what was built and what was not. What is not acceptable is presenting a simulated result as a measurement.

4. Tools, Components and Instruments

4.1 Software (all free)

Tool	Notes
LTspice	Recommended. Free, fast, best-supported, runs on Windows/macOS/Linux (via Wine). Nearly all online help you will find assumes it.

Tool	Notes
QUCS-S / Ngspice	Fully open source; good if you are on Linux. Same SPICE engine family.
C2S lab tools	We have a state of the art C2S lab here in our department. You can check the feasibility of doing your project there too, by contacting faculty in charge Dr.Nikhil
KiCad	Only if your project genuinely needs a PCB layout or a proper schematic drawing for the report. Not required.
Falstad Circuit Simulator (falstad.com/circuit)	Browser-based, animated, not accurate — excellent for *intuition* and for slides, never as a source of numbers. Say so if you use it.
Python + matplotlib, or a spreadsheet	For plotting measured data properly. Hand-drawn graphs on graph paper are also accepted if neat and correctly labelled.

On SPICE models: state which transistor model you used and where it came from. LTspice's default `2N2222` behaves differently from a real BC547B. If you build the circuit with a BC547, simulate it with a BC547 model — downloading the manufacturer's model is a five-minute job and it is part of doing this properly.

4.2 A standard component kit

The following covers Worked Example A, most of Example B, and the majority of the topic list. Assembled cost is typically ₹350–₹500 per team, and much of it may already be available in the lab store.

Category	Items
Active devices	BC547B ×10, BC557B ×10 (complementary PNP), 2N2222 ×5, BD139/BD140 pair ×2 (power, for Class AB), 1N4148 ×10, 1N4007 ×6, Zener 5.1 V and 6.2 V ×3 each, IRF540 or 2N7000 ×3 (MOSFET topics)
Passives	¼ W resistor assortment (5%), 10 kΩ and 100 kΩ potentiometers, ceramic caps 100 pF–0.1 µF, electrolytics 1 µF–1000 µF, a few 1% resistors if available
Power	8 Ω 5 W or 10 Ω 5 W wirewound resistor (as a loudspeaker substitute), small heatsinks with TO-220 mounting hardware
Build	Breadboard, jumper wire kit, crocodile leads, 9 V or 12 V DC adapter (regulated, ≥500 mA)

4.3 Instruments — and what to do without them

Lab bench slots will be published; you get scheduled access to the DSO and function generator. Outside those slots, the following substitutes are legitimate and you may use them, provided you state clearly in the report which instrument produced each number.

- **A digital multimeter is enough for all DC work** — Q-point verification, load and line regulation, ripple (on AC mV range, with care).
- **Your laptop's sound card is a genuine two-channel 20 Hz–20 kHz oscilloscope and signal generator.** Free software: Soundcard Scope, Visual Analyser, or Audacity for capture plus a spectrum plot. This is sufficient for audio-band frequency response, distortion measurement and FFT-based THD. **Always** couple it through a capacitor and a divider, never connect a laptop input directly to a circuit carrying more than about 1 V.

- **A phone tone-generator app** driving the headphone jack makes an adequate signal source below 20 kHz.
- **Measuring β yourself** takes two DMM readings and thirty seconds. Do it for every transistor you use, and put the number in your report. It is the single most useful measurement in this whole project.

The most important instrument limitation you must know

Most handheld DMMs specify AC voltage accuracy only up to a few hundred hertz, and many are badly wrong above 1 kHz. **You cannot build a frequency response plot out of DMM AC readings.** Every year several teams do, produce a beautifully smooth curve that rolls off at 2 kHz, and conclude their amplifier has a 2 kHz bandwidth. It does not; the meter does. Use the scope or the sound card for anything above a few hundred hertz.

5. Safety and Laboratory Rules

These are not optional, and they are short.

1. **No mains wiring. None.** Nobody in this course builds anything that plugs into 230 V. If your topic needs a DC supply, use a regulated adapter or a bench supply. If your topic involves a transformer, use a ready-made low-voltage adapter as your source and treat its output as your starting point.
2. **Set the bench supply's current limit before you connect anything.** 100 mA is plenty for small-signal work, 500 mA for power stages. This one habit will save most of your components.
3. **Check electrolytic capacitor polarity twice.** A reversed electrolytic vents, sometimes loudly, occasionally into your face. Take the two seconds.
4. **Anything dissipating more than about 250 mW needs a heatsink** and will be too hot to touch. Class A and Class AB output stages get hot by design; that is the topic, not a fault. Do not test with a finger.
5. **Discharge large capacitors before rewiring.** A 1000 µF cap charged to 12 V will make a memorable spark across a jumper wire.
6. **Power down before rewiring, every time.** Hot-plugging a breadboard is how transistors die.
7. **Never leave a powered circuit unattended,** especially one with a power transistor in it.
8. **Soldering only in the lab, under supervision,** with the extraction fan on. Most projects here need no soldering at all.
9. **Report any burn, smell or smoke immediately** — to the lab staff, not to the group chat. Nobody is penalised for a destroyed component. People are penalised for hiding it.

6. Policy on AI Tools and Academic Honesty

You may use ChatGPT, Claude, Copilot or similar tools while doing this project, under three conditions.

1. **Declare it.** The report has a short appendix listing which tools you used and for what. A truthful declaration costs no marks. An undeclared one that surfaces in the viva costs you the component.
2. **Own every value.** In the viva you may be pointed at any resistor in your schematic and asked why it has that value, and what happens if you double it. If you cannot answer, that part of the design is treated as not yours.

3. **Do not trust it on analog design.** This matters more here than in a programming course. Language models routinely produce bias networks that put the transistor in saturation, quote the wrong pinout for a BC547, confuse r_e with $r\pi$, drop the factor of 26 mV, and invent component values that satisfy no equation at all. **Check every number against Sedra–Smith or Boylestad, and against the datasheet.** The simulator is your friend here: if the AI's design is wrong, a five-second `.op` run will show you the transistor is in cut-off.

Fabrication — inventing measurements, photographing someone else's breadboard, drawing a waveform no instrument produced — is academic misconduct and is handled as such. Reporting a circuit that never worked is not.

7. Deliverables at a Glance

#	Deliverable	Contents	Due
D1	Abstract (1 page)	Title, team, specification you will meet, circuit topology, chosen mode, what you will measure, component list, references	15 Aug 2026
D2	Design file	Full hand calculations, load line, component selection with justification, predicted performance. Scanned handwritten pages are fine and preferred.	Reviewed at D3
D3	Progress presentation	8–10 slides, design file, simulation results, and whatever is built so far — with measured DC bias	14–19 Sep 2026
D4	Project folder	Schematics, SPICE files, measurement tables (raw), photographs of the build, logbook scan	30 Oct 2026
D5	Final report	12–18 pages including figures	30 Oct 2026
D6	Demonstration + viva	Live circuit or live simulation, 10 min talk, individual questions	27–29 Oct 2026

8. Timeline and Milestones

Twelve working weeks alongside your regular courses and lab sessions. The plan assumes about **3 hours per person per week** — roughly 35 hours per person in total. Scoped properly, that is enough. Compressed into October, it is not.

Week	Dates	What you should be doing	Milestone
W0	06 – 15 Aug	Form teams. Read the topic list. Pick a topic and write down the specification you intend to meet, in numbers. Do a first-cut hand design — even a rough one. Write the abstract.	D1 Abstract — 15 Aug
W1	17 – 22 Aug	Abstract feedback by 20 Aug. Install LTspice and simulate any textbook example end-to-end so you know the tool works. Order or draw components from the store this week — not in September.	Tools + parts sourced
W2	24 – 29 Aug	Complete the paper design: DC bias, load line, Q-point, every resistor justified. Small-signal predictions. Choose capacitor values from your cut-off targets.	D2 Design file
W3	31 Aug – 05 Sep	DC simulation. Confirm the Q-point matches your calculation. Sweep β and supply voltage to see how stable your bias really is.	Q-point verified in SPICE
W4	07 – 12 Sep	AC simulation: gain, bandwidth, impedances. First breadboard build. Measure DC voltages only — do not chase gain until the bias is right.	Bias measured on hardware

Week	Dates	What you should be doing	Milestone
W5	14 – 19 Sep	Progress presentation.	D3 Progress talk
W6	21 – 26 Sep	AC measurements: gain at mid-band, then the frequency response. First three-way comparison table.	First comparison
W7	28 Sep – 03 Oct	The troubleshooting week. Something will oscillate, distort, or refuse to bias. Leave room for it; this week is in the plan for a reason.	—
W8	05 – 10 Oct	Complete the measurement set. Run your sweeps (load, frequency, bias current, tolerance — whatever your topic demands).	Results complete
W9	12 – 17 Oct	Analysis. Explain every gap in the comparison table. Re-measure anything suspicious. Finalise all figures with axes, units and labels.	Figures frozen
W10	19 – 24 Oct	Write the report. Hardware freeze 24 Oct — after this, do not rebuild.	Draft report
W11	26 – 30 Oct	Demonstration and viva. Submit everything.	D5/D6 — 30 Oct

Two dates that decide the project

W1 — components. Every year a team loses three weeks waiting for a part. Source everything in the third week of August, including spares. Buy ten transistors, not three.

W4 — bias before gain. If the DC operating point is wrong, every AC measurement you take afterwards is meaningless. Get V_B, V_E and V_C to match your design within about 10% before you connect a signal generator.

9. Deliverable Specifications

9.1 D1 — Abstract (due 15 August)

One page, PDF. Filename `S3_AC_Abstract_<TeamNumber>.pdf`. Include:

- **Title**, specific. "CE Amplifier" is not a title. "Extraction of a Gummel–Poon Model for the BC547B From Measurement, and Evaluation of Its Predictive Accuracy for a Common-Emitter Amplifier" is.
- **Team** — names, roll numbers, intended division of work.
- **Specification in numbers** — this is the part we read most carefully. Supply voltage, gain, bandwidth, load, output power, regulation percentage, whatever your topic requires. Vague specifications produce vague projects.
- **Circuit topology** — a sketch or a description of the configuration you intend to use, and why that one.
- **Mode** — hardware, simulation, or both, with a sentence of justification.
- **What you will measure**, and with what instrument.
- **Component list** and rough cost.
- **References** — at least three, one of which must be a course textbook, and at least one datasheet.
- **The above-syllabus element** — one or two sentences naming what in this project goes beyond what the course teaches, and what you will have to read to get there. Abstracts without this are sent back.

The commonest feedback is "good topic, tighten the specification" or "good topic, halve it". Expect one of those.

Each team should Submit a hardcopy of the abstract to me by 15/08/2026 and also mail the softcopy to ameenudeen@cet.ac.in

9.2 D2 — Design File

The complete paper design, submitted at the progress review and included as an appendix to the final report. **Handwritten and scanned is preferred** — we want to see the working, not a typeset summary of it. It must contain:

- The DC analysis: assumed β and V_BE, divider currents, and the resulting V_B, V_E, V_C, I_C.
- The DC load line drawn on axes, with the Q-point marked, and a sentence on why you put it where you did.
- Small-signal parameters: g_m, r_e or $r\pi$, and the predicted gain, input impedance and output impedance.
- Capacitor selection: which capacitor sets which cut-off frequency, and the calculation for each.
- Predicted performance versus the specification, with a comment on any spec you expect to miss.
- A statement of what you assumed and what you neglected — this earns marks, not loses them.

9.3 D3 — Progress Presentation (14–19 September)

Fifteen minutes: about 8 minutes of slides, 3 minutes showing your circuit or simulation, 4 minutes of questions. Every member speaks. Bring the logbook and the design file.

1. Title, team, and your specification in numbers.
2. Circuit diagram, with the parts already built marked.

3. The key design equation, stated correctly, and how you used it.
4. Simulation results so far.
5. Measured DC operating point next to the designed one — a small table with two columns. This is the single slide we most want to see.
6. **The problem slide** — what is currently broken, wrong, or confusing. Compulsory. Teams claiming everything is fine get harder questions, not easier ones.
7. Plan for W6–W10.
8. One page of the logbook, showing a real debugging episode.

9.4 D4 — Project Folder

A shared folder or a zip, containing:

- Final schematic, clearly drawn, with every component value and the transistor part numbers marked.
- SPICE files (`.asc` and any `.lib`/`.mod` files you added) that open and run on the evaluator's machine.
- Raw measurement tables — the numbers as you recorded them, not just the processed graph. Include the instrument used and its settings.
- Photographs of the actual build: an overall view and one close-up where the wiring is legible.
- A scan or photographs of the logbook.

9.5 D5 — Final Report

Section	Content	Length
Abstract	Specification, what you built, headline result with a number	0.2 page
1. Introduction	Why this circuit, what question the project answers	1 page
2. Theory	Only the equations you actually use, with your notation defined. Do not reproduce a textbook chapter.	2–3 pages
3. Design	The full design procedure, in the order you did it, with calculations. Load line. Component table with justification for each value and the nearest standard value used.	3–4 pages
4. Simulation	Schematic, model used and its source, results, and any sweep you ran	2–3 pages
5. Measurement	Setup description, instruments, raw and processed results, photographs	2–3 pages
6. Comparison and analysis	The three-way table, and an explanation of every gap in it. The most important section in the report.	2–3 pages
7. Troubleshooting	What went wrong and how you found it. At least one episode, written honestly.	1 page
8. Conclusion and limitations	What you now know; what you would do differently	0.5 page

Section	Content	Length
References + Appendices	IEEE style, min. 6 including one datasheet. Appendix A: design file. Appendix B: contribution statement, signed. Appendix C: AI declaration.	—

Figure standards — marks are lost here routinely. Every axis labelled with quantity and unit. Frequency response on a log frequency axis with gain in dB. Simulated and measured curves on the *same* axes wherever both exist. Every schematic legible with values marked. Oscilloscope photographs must have the volts/div and time/div stated in the caption. No photographs of a screen taken at an angle in a dark room.

9.6 D6 — Demonstration and Viva (27–29 October)

Twenty-five minutes per team: 10 minutes presentation, 6 minutes live demonstration, 9 minutes of individual questions. If you built hardware, bring it powered and working — or bring it not working and be ready to explain what you know about why. Sample viva questions:

- "Point at the resistor that sets your Q-point. What happens to V_CE if I double it?"
- "Your bypass capacitor is 100 µF. Why not 10 µF? Why not 1000 µF?"
- "Measure V_BE for me right now. Is that what you assumed in the design?"
- "Your measured gain is 15% below the simulated one. Give me the two largest contributors, in order."
- "What would happen if I removed the emitter resistor entirely? Try it."
- "Which transistor parameter did your design depend on most sensitively, and how do you know?"

10. Evaluation Rubric (15 marks)

Criterion	Marks	What earns full marks
Individual understanding (viva)	4	Every member can justify the design choices, explain the measurements, and reason about changes to the circuit on the spot.
Design quality, rigour and reach	3	Every component value traced to a calculation; assumptions stated; Q-point correct. Full marks require the project to have genuinely gone beyond the syllabus — evidence of reading past the course and of a question the lecture notes do not answer.
Effort and process (logbook, progress, response to feedback)	3	Dated entries across all twelve weeks, failures recorded, review feedback visibly acted on.
Comparison and analysis	3	Three-way table complete; every discrepancy explained with a named mechanism and, where possible, a number.
Report, figures and demonstration	2	Clear structure, legible schematics, proper axes, working demo, all members contributing.
TOTAL	15	

Note what is **not** in the table: there are no marks for the circuit meeting its specification, no marks for hardware over simulation, and no marks for how complicated the circuit is.

Penalties

−3 No logbook, or one clearly written retrospectively.

−2 Component values with no supporting calculation anywhere.

−2 SPICE files that do not run, or measurements with no stated instrument.

−2 Missing or false AI-use declaration.

Zero, and referral for copied designs presented as original, or fabricated measurements.

Late: 2 marks per day up to three days; nothing accepted after 2 November.

11. Working as a Team

A workable split for three, and the one we recommend:

- **Member A — Design and theory.** Owns the design file, the calculations, the load line, the choice of topology. Answers "why this value".
- **Member B — Simulation.** Owns the SPICE schematic, the model selection, the sweeps and the tolerance study. Answers "what does it predict".
- **Member C — Build and measurement.** Owns the breadboard, the instrument setup, the raw data and the photographs. Answers "what does it actually do".

Every member owns the report section corresponding to their role, and the comparison section is written jointly. **Rotate once:** in Week 6, have each member spend one session doing someone else's job, with that person watching. Record it in the logbook. It is the cheapest possible insurance for your viva marks.

If a member stops contributing, raise it at the progress review, not in the last week. The contribution statement is signed by all members and evaluators may award differentiated marks.

12. Worked Example A — A Depth Project

A complete specification at the depth and scale we expect. It is the topic listed at **P1**. You should use this as a template for scoping your own project. Section 13 gives a **breadth** example of the opposite kind; read both before deciding.

Know Your Transistor: Building a Device Model From Your Own Measurements, and Testing It Against a Real Amplifier

12.1 The question

Every design calculation you have ever done in this course rests on three borrowed numbers: β, V_BE and — if you were being careful — r_o. Where do they come from? The datasheet gives β as a range spanning better than two to one. V_BE is "about 0.7 V". The simulator's default `NPN` is a generic device that corresponds to nothing on your breadboard.

So the project asks: **if you measure your own transistor properly and build your own SPICE model from those measurements, does your amplifier become predictable?** You will characterise a real BC547 over four decades of current, extract its saturation current, ideality factor, current-dependent β and Early voltage, write your own model card, and then settle the question by experiment — simulating the same amplifier with a generic model, with a manufacturer model, and with your own, against what the bench actually says.

The result is a number that answers something every student in this course silently wonders: **how much of the gap between calculation and reality is just not knowing your device?**

12.2 Why this is a good project

- **It starts inside the syllabus and finishes outside it.** The starting point is Module 1 biasing and the Module 2 hybrid-π model — nothing else. The destination — Gummel plots, ideality factor, β roll-off at high and low injection, Early voltage extraction, SPICE model-card fitting — is second-year-accessible but is not lecture material. That is exactly the intended altitude.
- Maps to theory **CO1 and CO2**, lab **CO1–CO3**, all at K3, and pushes into K4 in the analysis.
- **It needs almost no equipment.** The bulk of the work is a DMM, a handful of resistors and a power supply. The AC section needs a sound card. Total component cost is under ₹150.
- It changes how you read a datasheet for the rest of your degree, which is a larger return than most projects offer.
- It fails gracefully: the extraction half is a complete project on its own if the amplifier half runs out of time.

12.3 Specification

Item	Target	Notes
Device under study	BC547B, 10 devices from one batch	Buy from a single source so the batch statistics mean something

Item	Target	Notes
I_C range characterised	10 µA to 20 mA (three-plus decades)	The interesting behaviour is at the ends, not the middle
Parameters extracted	I_S, ideality factor n, β(I_C), V_A (Early), r_o	Each with a stated uncertainty
Model deliverable	A SPICE `.model` card you wrote	Fitted to your data, not copied
Test amplifier	CE stage, I_C = 1 mA, $\|A_v\| \approx 40$, V_CC = 12 V	Deliberately the standard design, so the comparison is clean
Headline metric	Prediction error in A_v for three models	Generic NPN / manufacturer BC547 / your extracted model
Instruments	DMM throughout; sound card for the AC measurements	Base current measured as the drop across a known series resistor

12.4 Stage-by-stage plan

Weeks	Stage	What you do and what you must verify
W2	Stage 0 — Design and predict	Design the CE test amplifier on paper using datasheet-typical values, and write down your predicted I_C, V_CE and A_v. Sign and date it. This is your control: at the end of the project you will know exactly how wrong the datasheet route was. Also design the measurement fixtures — the series resistors that let you read I_B and I_C as voltages.
W3	Stage 1 — The forward Gummel measurement	Fix V_CE at 5 V with a supply and a resistor. Step V_BE from about 0.40 V to 0.75 V and record I_C and I_B at each point. Technique: put a 100 kΩ resistor in the base and a 1 kΩ in the collector, and measure the voltage across each — that gives you microamps and milliamps on the same meter. Verify: plot ln(I_C) against V_BE. Over the middle decades it must be a straight line. Extract the slope (which gives n·V_T) and the intercept (which gives I_S). If it is not straight anywhere, your measurement is wrong, not the transistor.
W4	Stage 2 — β and the output characteristics	From the same dataset, plot β = I_C/I_B against I_C on a log axis. It will rise, peak and fall — three regions, three different physical causes. Then measure the output family: for I_B = 5, 10, 15, 20 µA, sweep V_CE from 0.2 V to 10 V and record I_C. Verify: the curves are not flat. Extrapolate them backwards to the V_CE axis; they converge near −V_A. Extract the Early voltage and compute r_o at your intended operating point.
W5	Progress review	Present the Gummel plot, the extracted I_S and n, and the β curve. A completed extraction is a strong W5 position.
W6	Stage 3 — Building the model	Write a `.model` card with your extracted IS, NF, BF, VAF, and IKF for the high-current β roll-off. Simulate the same Gummel measurement in SPICE and overlay it on your measured data. Adjust and repeat until they agree. Verify: your simulated Gummel plot lies on your measured points across at least three decades. Doing the fit

Weeks	Stage	What you do and what you must verify
		by least squares in ten lines of Python is a legitimate and welcome approach; doing it by eye and iteration is equally acceptable if you document the iterations.
W7	Stage 4 — The test amplifier	Build the CE stage using a transistor you personally characterised. Measure the Q-point, then the mid-band gain, then the output impedance. Then do the measurement that makes the project: sweep the bias current from about 0.2 mA to 5 mA (by changing R_E and the divider) and measure the gain at each point.
W8	Stage 5 — The three-model shoot-out	Simulate that same bias sweep three times: with LTspice's generic `NPN`, with the manufacturer's BC547B model, and with your own. Plot all three predictions against your measured gain-versus-bias-current curve. This is the headline figure of the report. Quantify each model's mean prediction error.
W9	Stage 6 — Batch statistics	Repeat the β extraction (at one current — this takes two minutes per device once the fixture exists) for all ten transistors. Histogram the results. Then ask the design question: given this measured spread, how much does your Q-point actually move? And how much does your input impedance move? The two answers are not the same, and the difference is the point.
W10	Stage 7 — Analysis and writing	Answer the questions in 12.6.

12.5 Required figures

1. The Gummel plot: ln(I_C) and ln(I_B) against V_BE, measured points with fitted straight lines, and the extracted I_S and n annotated on the figure.
2. β against I_C on a log current axis, over your full measured range, with the three regions marked and the datasheet's typical curve overlaid for comparison.
3. The output characteristic family, with the backward extrapolation drawn and the Early voltage marked on the negative V_CE axis.
4. Your fitted model's simulated Gummel plot overlaid on your measured points, showing the quality of the fit.
5. Histogram of β across ten devices from one batch, with mean and standard deviation stated, and the datasheet's guaranteed range drawn as a band.
6. **The headline figure:** measured amplifier gain versus bias current, with the three model predictions overlaid as lines.
7. Measured amplifier frequency response with the three simulated responses overlaid.
8. The three-way comparison table for I_C, V_CE, A_v, Z_out — but with **five** columns here: designed-from-datasheet, simulated-generic, simulated-manufacturer, simulated-your-model, measured.

12.6 The analysis questions you must answer

1. What ideality factor n did you extract? Ideal diode theory says 1. State your value, its uncertainty, and — if it differs — name a mechanism that could explain the difference.

2. At the high-current end your ln(I_C) plot bends away from the straight line. Identify the two candidate causes (one inside the device, one in your measurement) and design a check that distinguishes between them. Run it.
3. β falls at both low and high I_C. Give a physical mechanism for each end. At what current is β maximum for your device, and is that where you biased your amplifier? If not, should it have been — what else would have changed?
4. Compute r_o at your operating point from your extracted Early voltage. What fraction of your amplifier's gain error is accounted for by having ignored r_o in the original hand design? Show the arithmetic.
5. Rank the three SPICE models by prediction error against your measurements. For the worst one, identify **which single parameter** is most responsible, and support that claim by changing only that parameter in the model and re-simulating.
6. From your batch histogram: mean β, standard deviation, and the range. Your original design assumed a single value. What percentage of the ten devices, dropped into your circuit unchanged, would give a Q-point within 10% of target? Compute it from your data, then verify it by actually swapping devices.
7. Your voltage-divider bias makes I_C largely insensitive to β. Does it make the **gain** insensitive? Does it make the **input impedance** insensitive? Quantify all three from your own measurements, and explain why the three answers differ.
8. What, specifically, did the datasheet fail to tell you that you needed? Answer as an engineer writing a note to next year's students.

12.7 Effort estimate

For a team of three: about 8 person-hours on the design and fixtures, 20 on the Gummel and output-characteristic measurements (this is the patient, repetitive part — share it out), 15 on model fitting, 15 on building and measuring the amplifier, 10 on the three-model comparison, 8 on batch statistics, and 22 on analysis, writing and slides. Roughly **95–100 person-hours** over twelve weeks.

The risk here is boredom, not difficulty. Taking sixty DMM readings is tedious and it is where teams cut corners. Two mitigations: split the sweep across three people in one sitting, and — if you have the appetite — automate it, which is topic **P20** and a legitimate extension of this project.

12.8 If you finish early

- Extract the temperature coefficient of V_BE by repeating a single-point measurement at several temperatures (a hair dryer and a freezer spray span a useful range), and add TNOM and XTI behaviour to your model.
- Extract f_T indirectly using the Miller technique: add a known base-collector capacitor, measure the resulting f_H, and back out the device's own C_μ.
- Characterise a BC557 PNP as well and build a matched-pair model, which feeds directly into Worked Example B.
- Run the same extraction on a MOSFET — V_th, k_n, channel-length modulation — and compare how much more or less predictable the two device families are.

13. Worked Example B — A Breadth Project

Example A studies one thing very hard. This one assembles four modules' worth of syllabus into a single circuit that the syllabus does not contain, and then studies what happens at the edge of stability. It is the topic listed at **P2**.

The trade-off is real. A breadth project has more blocks, so more can break, and no single block is analysed as deeply. What it gives you in return is the experience of building something recognisably *general-purpose* out of parts you designed yourself — and of meeting, for the first time, the problem that dominates real amplifier design and appears nowhere in your syllabus: an amplifier with too much feedback oscillates.

A Discrete Operational Amplifier: Assembling the Syllabus Into Something the Syllabus Does Not Contain

13.1 The question

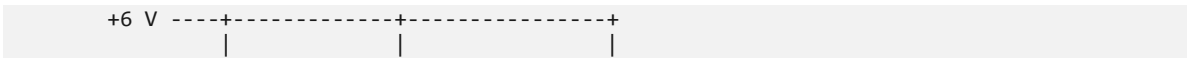
You have studied biasing, the CE amplifier, negative feedback and the class AB output stage as four separate topics. Stack them and you have an operational amplifier — the component that every later course will hand you as a black triangle. This project builds one from discrete transistors, characterises it as a device in its own right, and then uses it to test the four claims Module 3 makes about negative feedback: that it reduces gain, extends bandwidth, reduces distortion, and modifies input and output impedance.

Then comes the part that is not in the syllabus, and which is the real destination. Close the loop hard enough and your amplifier will ring, and then oscillate. **Why does an amplifier with more negative feedback become unstable?** You will measure the phase margin from your own step response, add a compensation capacitor, and map the trade between stability and bandwidth. That trade is the central fact of practical amplifier design, and you can discover it in second year with three transistors and a sound card.

13.2 Why this is a good project

- **Every block comes from the syllabus; the assembly does not.** Biasing and current sources (Module 1), the CE gain stage and its high-frequency behaviour (Module 2), all four feedback effects (Module 3), the class AB output stage (Module 4). The differential pair, the current mirror, open-loop versus closed-loop characterisation, phase margin and Miller compensation are the above-syllabus content — and each is reachable from what you already know.
- Maps to theory **CO1–CO4** and lab **CO1–CO3**.
- It makes Module 3 quantitative. Rather than being told feedback extends bandwidth, you will measure gain–bandwidth conservation across three closed-loop gains on your own amplifier.
- Cheap: about eight small-signal transistors, one complementary output pair, and passives. Under ₹200.
- It decomposes cleanly. The differential pair alone, fully characterised, is a complete project. So is the two-stage amplifier without the output buffer.

13.3 The architecture



```
          [current      [ CE GAIN         [ CLASS AB
           mirror        STAGE ]           BUFFER ]
           load ]            |            BD139/BD140
              |              |                |
in+ --[ DIFFERENTIAL ]--+   +---||---+       +---- out
in- --[   PAIR       ]  |   |   Cc   |       |
              |         |   +--------+       |
         [ tail current                       |
           mirror ]                           |
              |                               |
     -6 V ----+-------------------------------+

Stage 1: differential pair, current-mirror tail and load
Stage 2: common-emitter voltage gain stage
Stage 3: class AB complementary output buffer
Cc     : Miller compensation capacitor  <-- your main variable
```

13.4 Specification

Parameter	Target	Notes
Supply	±6 V	Two 9 V batteries with a common centre node, or a split adapter arrangement. Never mains.
Open-loop gain	≥ 60 dB (×1000)	Modest by op-amp standards, and entirely achievable with two stages
Input offset voltage	Measure it; expect 5–50 mV	Discrete transistors are unmatched. The offset is a result, not a defect.
CMRR	≥ 50 dB with the current-mirror tail	Also measure it with a plain tail resistor, for the comparison
Output	±3 V into 1 kΩ	Deliberately modest — keeps dissipation and risk low
Compensation	C_c adjustable: 0, 10 pF, 47 pF, 220 pF, 1 nF	Your principal independent variable
Closed-loop gains tested	×100, ×10, ×1	Unity gain is where it will misbehave, which is the point
Instruments	DMM, sound card scope and generator	Step response via a square wave from the sound card

13.5 Stage-by-stage plan

Weeks	Stage	What you do and what you must verify
W2	Stage 0 — Design	Design all three blocks on paper: tail current, differential-pair bias, mirror ratio, CE stage gain, output-stage quiescent current, and the dissipation of every device. Verify: predicted open-loop gain as the product of the two stage gains, with the loading between them accounted for.
W3	Stage 1 — Differential pair, simulated	Simulate the DC transfer characteristic (V_out against differential input) and the common-mode rejection, once with a tail resistor and

Weeks	Stage	What you do and what you must verify
		once with a current mirror. Verify: the mirror version's CMRR is far higher, and you can point at the tail impedance as the reason.
W4	Stage 2 — Differential pair, built	Build it. Measure the DC transfer curve point by point — this is a beautiful measurement and it takes twenty minutes. Measure the input offset voltage, then measure V_BE of the two input transistors separately at equal current and check whether their mismatch predicts the offset you saw. Measure differential gain, common-mode gain and hence CMRR, both with a tail resistor and with the mirror.
W5	Progress review	A characterised differential pair with a measured CMRR comparison is a strong W5 position and needs no apology.
W6	Stage 3 — Adding the gain stage	Add the CE stage. Now measure the open-loop gain — which requires care, because a 60 dB amplifier saturates on a millivolt of offset. Technique: drive it through a 1000:1 resistive attenuator so your generator's minimum output becomes microvolts at the input, and null the offset with a trimmer. Document this technique in the report; working out how to measure a quantity is engineering.
W7	Stage 4 — Output buffer	Add the class AB stage and set its quiescent current. Verify: the amplifier drives 1 kΩ without the gain falling. Expect trouble: this is the week it will probably start oscillating. Do not fix it yet — characterise it. What frequency? Does it depend on the load? On the closed-loop gain? Record everything; this is your best troubleshooting episode.
W8	Stage 5 — Closing the loop	Configure for closed-loop gains of 100, 10 and 1. At each: measure gain, bandwidth, THD, input impedance and output impedance. Verify all four Module 3 predictions numerically — particularly that gain × bandwidth stays roughly constant across the three configurations.
W9	Stage 6 — Compensation and stability	Feed a small square wave and capture the step response for each value of C_c. Measure the percentage overshoot and the ringing frequency; convert overshoot to damping ratio and hence to an estimated phase margin. Then plot closed-loop bandwidth and phase margin against C_c on the same axes. This is the headline figure.
W10	Stage 7 — Analysis and writing	Answer the questions in 13.7.

13.6 Required figures

1. Measured DC transfer characteristic of the differential pair, V_out against differential input, with the linear region and the saturation limits marked.
2. CMRR against frequency, measured, for the resistive tail and the current-mirror tail on one set of axes.
3. Open-loop gain Bode plot — magnitude and, from simulation, phase — with the measured points overlaid on the simulated curve.
4. Closed-loop frequency response at gains of 100, 10 and 1, on one plot, with the gain–bandwidth product annotated for each.

5. THD against loop gain, with the 1/(1+Aβ) prediction overlaid.
6. Input and output impedance, open-loop and closed-loop, as a table and as a bar chart.
7. Step response captures at five values of C_c, showing the progression from oscillation through ringing to overdamped.
8. **The headline figure:** closed-loop bandwidth and estimated phase margin against compensation capacitance, on twin axes, with your chosen operating point marked.
9. The three-way comparison table for open-loop gain, CMRR, offset, bandwidth, output swing and slew rate.

13.7 The analysis questions you must answer

1. Your input offset voltage is some tens of millivolts. Measure the V_BE mismatch of your two input devices directly and calculate the offset it predicts. Does it account for what you measured? If not, name another contributor and estimate its size.
2. Replacing the tail resistor with a current mirror improved CMRR by a measured amount. Explain the mechanism in terms of tail impedance, and check whether the measured improvement is consistent with the impedance ratio you would estimate.
3. Verify gain–bandwidth conservation across your three closed-loop gains. State the deviation. At which gain does the relationship break down first, and why?
4. Compare your measured THD reduction against the 1/(1+Aβ) prediction. Where the agreement is poor, say what the theory assumes that your amplifier violates.
5. From the overshoot in your uncompensated step response, estimate the damping ratio and hence the phase margin. Compare with the phase margin your simulation reports. Explain any disagreement.
6. Explain what the Miller compensation capacitor does to the two dominant poles of the amplifier. Why is it connected **across** the gain stage rather than from that node to ground? Confirm your explanation by simulating both arrangements.
7. Measure the slew rate. Relate it quantitatively to the tail current and the compensation capacitor. Then predict the slew rate for a different C_c and verify your prediction by measurement.
8. Your amplifier has an open-loop gain of roughly 10^3; a 741 has roughly 10^5 and a modern part 10^6. Name three specific things you would change to close that gap, and state what each would cost you — in current, in stability, or in complexity.

13.8 Effort and scoping

For a team of three: about 12 person-hours on the paper design, 20 on the differential pair including the transfer-curve measurement, 18 on the gain stage and the open-loop measurement technique, 15 on the output buffer and the oscillation episode, 18 on the closed-loop measurements, 15 on the compensation study, and 22 on analysis and writing. Roughly **110–120 person-hours** — this is the more demanding of the two examples, and teams choosing it should be confident about their lab access.

The scoping rule is absolute here: characterise each block completely before connecting the next one. A three-stage amplifier where all three blocks are unverified is not debuggable, and teams that skip this discover it in the second week of October. If you fall behind, the correct move is to drop the output buffer and present a fully characterised two-stage amplifier — that is a complete and creditable project.

13.9 If you finish early

- Add a current-mirror active load to the differential pair and measure how much the open-loop gain rises.
- Build a second copy and measure the unit-to-unit spread in offset, gain and bandwidth — which connects directly to Example A's batch statistics.
- Use your op-amp to build something: an active filter, a precision rectifier, a Schmitt trigger — and characterise how your amplifier's limitations show up in that application.
- Add an input-offset nulling trim and measure the residual drift with temperature.
- Deliberately reduce the phase margin below zero and characterise the resulting oscillator — amplitude, frequency and waveform — as a circuit in its own right.

14. Suggested Topics

Every topic below starts from something you have studied and goes somewhere you have not. That is the design rule for this project, and it is worth stating plainly:

> **What separates a project from a lab experiment**
>
> Your lab sheet says: *design a CE amplifier for a specified gain and plot its frequency response*. That is a valuable exercise and you will do it in the lab. It is **not** a project, because the answer is known, the method is given, and nothing about it can surprise you.
>
> A project takes the same circuit and asks a question nobody has handed you the answer to: how does its distortion depend on where you biased it? How much of its unpredictability comes from not knowing the device? What happens when you wrap enough feedback around it to make it unstable? **The circuit can be familiar. The question must not be.**

The **Mode** column shows what we think suits each topic: **H** hardware, **S** simulation, **B** both. It is a recommendation, not a rule. **Builds on** names the syllabus material you start from; the topic description says where you go from there.

#	Topic	Where it starts, and where it goes	Mode	Builds on
P1	Device Characterisation and Model Extraction (worked example, §12)	Starts from biasing and the hybrid-π model. Goes to Gummel plots, ideality factor, β roll-off, Early voltage and writing your own SPICE model card — then tests whether it predicts a real amplifier better than the stock models do. Fully specified in Section 12.	B	M1, M2
P2	A Discrete Operational Amplifier (worked example, §13)	Starts from four separate syllabus blocks. Goes to differential pairs, current mirrors, open-loop characterisation, phase margin and Miller compensation. Fully specified in Section 13.	B	M1–M4
P3	Build an Instrument: a sound-card transistor curve tracer	Starts from the output characteristics you plot point-by-point in the lab. Goes to building a circuit that sweeps base current and collector voltage automatically and displays the full family live, then using your instrument to characterise twenty devices and study the batch spread. You end the semester owning a tool, which is an unusual outcome for a second-year project.	H	M1
P4	Noise: the floor beneath every amplifier	Starts from the CE amplifier you already know. Goes to the topic the syllabus never mentions: thermal and shot noise, input-referred noise voltage and current, noise figure, and the existence of an optimum source resistance at which your amplifier is quietest. Measure the noise floor with a sound-card FFT, verify the 4kTR law on plain resistors first, then characterise your amplifier and find its optimum experimentally.	B	M2

#	Topic	Where it starts, and where it goes	Mode	Builds on
P5	Distortion as a measurable quantity	Starts from the exponential I–V relation in your first lecture. Goes to predicting the second-harmonic distortion of a CE stage analytically from that exponential, verifying that HD2 grows linearly with signal amplitude, showing how it depends on where you biased, and then killing it with negative feedback and checking the reduction against 1/(1+Aβ). Turns three syllabus topics into one continuous quantitative story.	B	M2, M3
P6	Why Good Amplifiers Oscillate: stability and compensation	Starts from the feedback amplifier in Module 3. Goes to the question Module 3 does not ask: what happens when the loop gain is large and the phase shift reaches 180°? Build a three-stage amplifier, wrap feedback around it, watch it oscillate, measure the phase margin from the step response, and tame it by dominant-pole and lead compensation. Map the stability-versus-bandwidth trade.	B	M2, M3
P7	The Differential Pair and the Current Mirror	Starts from single-transistor biasing. Goes to the two building blocks that every integrated analog circuit is made of and that your syllabus stops just short of: measure the tanh transfer characteristic, the offset arising from device mismatch, CMRR with resistive versus active tail, and the gain boost from an active load.	B	M1, M2
P8	Making a Reference That Does Not Care About Temperature	Starts from $V_{BE} \approx 0.7$ V and the Zener regulator. Goes to the fact that V_{BE} drifts about −2 mV/°C while the thermal voltage rises: build a PTAT current source, then a discrete bandgap-style reference that cancels the two, and measure the temperature coefficient of each against a plain Zener over a 40 °C range. Cancellation you can measure.	B	M1, M4
P9	A Photodiode Front-End: the four-way trade nobody warned you about	Starts from the CE amplifier and negative feedback. Goes to a real design brief: convert a photodiode's microamps to volts, where gain, bandwidth, noise and stability are in direct conflict, and where the sensor's own capacitance is what makes the amplifier ring. Design it, build it, measure the trade, and add the compensation capacitor that fixes it.	B	M2, M3
P10	Switching versus Linear: a discrete buck converter	Starts from the series regulator in Module 4, which wastes the difference as heat. Goes to the alternative the syllabus lists but does not analyse: build a simple discrete buck converter, measure efficiency against output current for both approaches, and quantify what switching costs in ripple, noise and complexity. The crossover point is the result.	B	M4
P11	An Automatic Gain Control Loop	Starts from the amplifier and the feedback structure. Goes to a control system: a detector, a loop filter and a variable-gain element (JFET or LED–LDR) that holds the output constant as the input varies over 40	B	M2, M3

#	Topic	Where it starts, and where it goes	Mode	Builds on
		dB. Measure the attack and release dynamics, the loop's stability, and what happens when you make it too fast.		
P12	The Wien Bridge as a Nonlinear System	Starts from the Barkhausen criterion and the oscillator you build in the lab. Goes past the point where the lab sheet stops: with fixed gain it either dies or clips, so what actually determines the amplitude? Study start-up transients, the limit cycle, and three amplitude-control schemes (diode, thermistor, JFET) compared on settling time, amplitude stability and THD. Nonlinear dynamics, reachable with three components.	B	M3
P13	A Tuned Amplifier and a Voltage-Controlled Oscillator	Starts from the RC-coupled amplifier and the LC oscillator. Goes to resonance and selectivity: design a tuned amplifier for a specified Q and centre frequency, measure the actual Q and account for the loss, then add a varactor to a Colpitts oscillator and characterise the tuning curve, its linearity, and frequency pulling under load.	B	M2, M3
P14	Computing With the Exponential: log, antilog and a multiplier	Starts from the same I–V relation as P5, but exploits it rather than fighting it. Goes to logarithmic and antilogarithmic amplifiers and then to a discrete analog multiplier built from them — a circuit that performs arithmetic in continuous time. Characterise accuracy, dynamic range and temperature sensitivity, and explain why the last one is the hard part.	B	M1, M2
P15	An Analog Computer: solving a differential equation in hardware	Starts from RC integrators in Module 1. Goes to using several of them, with summing and scaling, to solve a second-order differential equation continuously — a damped oscillator, or a predator–prey system — and comparing the circuit's trajectory against a numerical solution. Historically how computing was done; conceptually a striking demonstration of what analog circuits *are*.	B	M1, M3
P16	A Chaotic Oscillator	Starts from the oscillator criteria in Module 3. Goes to what happens when you add a nonlinear negative resistance: build Chua's circuit or a comparable chaotic oscillator, capture the attractor in XY mode, and map the route from a stable limit cycle through period doubling into chaos as one parameter varies. Demanding, spectacular, and entirely within reach of discrete components.	B	M3
P17	Thermal Runaway: when a circuit destroys itself	Starts from the class AB output stage. Goes to the failure mode the syllabus mentions in passing: quiescent current rises with temperature, which raises dissipation, which raises temperature. Measure the loop experimentally, determine the thermal time constant, then design against it by	B	M4

#	Topic	Where it starts, and where it goes	Mode	Builds on
		thermally coupling the bias network to the output devices and prove the fix by measurement.		
P18	Bootstrapping and Impedance Enhancement	Starts from the input impedance limits of a CE stage. Goes to the techniques that beat them: bootstrapped bias networks, active loads and Darlington configurations. Measure input impedance directly (the substitution method is itself worth learning), and quantify how far past the plain-circuit limit each technique gets you, and what it costs.	H	M2
P19	A Real Design Brief: a low-noise microphone or piezo preamplifier	Starts from the RC-coupled amplifier. Goes to designing against a full specification rather than a single number — source impedance, noise floor, headroom before clipping, frequency response, and gain — for a sensor with an awkward output. Measure whether you met each specification. The most industry-like project on this list.	B	M2, M3
P20	Automating the Bench: a measurement and model-fitting rig	Starts from the measurements everyone takes by hand. Goes to a Python-plus-sound-card system that sweeps frequency or bias automatically, captures the response, and fits the hybrid-π model parameters to the data by least squares. Then use it to characterise a circuit far more thoroughly than manual measurement allows. Pairs naturally with P1.	B	Any
P21	Tolerance, Yield and Worst-Case Design	Starts from a design that works on your breadboard. Goes to the manufacturer's question: over 5% resistors, 20% electrolytics, β spanning 100–400 and 0–60 °C, what fraction of assembled units meet the specification? Monte-Carlo in SPICE, then test the prediction by building the same circuit five times from different components and measuring the spread.	B	Any
P22	Distortion as a Design Goal: harmonic engineering in a guitar pedal	Starts from diode clipping and the CE gain stage. Goes to treating distortion as the deliverable rather than the defect: how symmetric versus asymmetric clipping changes the harmonic structure, how the drive level moves the spectrum, and why two circuits with the same THD sound different. Rigorous harmonic analysis wearing a fun hat.	H	M1, M2

Proposing your own. Welcome, and the test is the one in the callout above: name the circuit you start from, and name the question about it that you cannot currently answer. If you can do both in two sentences, bring it to me by 15th August.

15. Choosing and Scoping Your Topic

Four questions before you commit:

1. **Does my project ask a question the course does not answer?** Name the circuit you start from and the question about it you cannot currently answer. If the question is one your lab sheet already answers, choose again — see the callout in Section 14.
2. **Can I write the specification as numbers?** "A gain of 40 into 10 kΩ with f_L below 100 Hz from a 12 V supply" is a project. "Study CE amplifiers" is not. If you cannot fill in numbers at the abstract stage, you have not chosen a topic yet.
3. **Is there something I can calculate, and then check?** If no quantity in your project can be predicted on paper, you have no way of knowing whether your circuit is right — and neither do we.
4. **Does the first block work on its own?** Structure the project so that if the ambitious part fails, you still have a complete, defensible result. Both worked examples are built this way.
5. **Have I checked the components exist in the store or the market?** Do this in Week 0, not Week 5. Substituting an unavailable transistor after you have designed around its parameters means redoing the design.

On scope: the commonest failure in this project is over-ambition, not laziness. A team proposes a four-stage amplifier with a regulated supply and an oscillator in August, and demonstrates a half-biased first stage in October. **Halve your plan at the abstract stage.** Sections 12.8 and 13.9 show what extension looks like, and an extension is always better received than an unfinished ambition.

A second-year-specific warning: analog circuits punish vagueness in a way that programming does not. A program with a wrong constant still runs. An amplifier with a wrong bias resistor produces a flat line, and you cannot debug it by reading the output. Get the paper design right first — it is the cheapest hour you will spend.

16. Common Pitfalls

Collected from previous experiences. Most teams hit at least four of these; the ones who read this list in August hit fewer.

Pitfall	How to avoid or detect it
Transistor pinout wrong	BC547 is C–B–E viewed from the flat face; 2N2222 in TO-92 is E–B–C; the metal-can version differs again. Symptom: V_B near 0.3 V and nothing works. Check the datasheet every single time, and test with the DMM's diode range before inserting.
Building the frequency response from DMM AC readings	Most handheld meters are inaccurate above a few hundred hertz. Symptom: a beautiful roll-off at 1–2 kHz that is entirely the meter. Use the scope or the sound card above 200 Hz.

Pitfall	How to avoid or detect it
Measuring gain with the output clipping	Symptom: gain that falls as you increase the input. Always look at the output waveform before recording a gain number. Start with an input of a few millivolts.
No common ground	Signal generator ground, scope ground, supply ground and circuit ground must all be one node. Symptom: enormous mains hum, or readings that change when you touch the board.
Forgetting the emitter bypass capacitor	Symptom: measured gain roughly R_C/R_E instead of the designed value — often 10× too small. It is a diagnostic ratio worth remembering.
Assuming β from the datasheet	Datasheet β for a BC547B spans 200–450. Measure it. Two minutes with a DMM saves a week of confused analysis.
Assuming V_BE = 0.7 V and never checking	Measure it at your actual I_C. It is often 0.62–0.68 V, and the difference matters in your bias arithmetic.
Electrolytic reversed or coupling capacitor polarity wrong	Check every one. In a coupling position the DC voltage on each side determines the orientation — work it out rather than guessing.
High-gain stage oscillating	Symptom: output looks like noise, or there is a signal with no input. Causes: long breadboard leads, no supply decoupling, output wire running next to the input wire. Fix: add 0.1 µF from supply to ground *at the transistor*, shorten leads, separate input and output physically. Then write it up — it is exactly the troubleshooting episode the report asks for.
SPICE model mismatch	Simulating a generic `NPN` and building with a BC547 will not agree, and the disagreement is not physics, it is bookkeeping. Download the manufacturer's model and say which one you used.
Breadboard contact resistance and stray capacitance	At high frequencies a breadboard is not a wire. If your measured f_H is far below simulation, suspect this before suspecting the transistor.
Power transistor with no heatsink	Symptom: works for thirty seconds, then the bias drifts, then it fails. Calculate the dissipation *before* building, in Stage 0.
Everything left to October	The logbook makes this visible and it is explicitly penalised. W7 is where projects are actually decided.

17. Frequently Asked Questions

Question	Answer
We have very little lab access. Can we do this?	Yes. Take the simulation route with the tolerance study, or the hybrid path: breadboard and DC-measure what you can with a multimeter at home, simulate the rest. Say clearly what was done which way.
Is a hardware project worth more marks than a simulation one?	No. The rubric in Section 10 makes no distinction. The extra requirement on simulation-only projects (Section 3) exists precisely so that the routes are equally demanding.

Question	Answer
Our circuit never worked. Are we going to fail?	No — provided you can show what you tried, what you measured, and what you concluded. Section 6 of the report is for exactly this. A well-diagnosed failure scores in the upper band. Concealing it does not.
Can we use an op-amp?	Not as the core of the project. This course is about discrete transistor circuits and that is where the marks are. An op-amp in a supporting role — as a buffer for a measurement, say — is fine if you say so.
Can two teams take the same topic?	Yes, up to two teams per topic. Your designs and measurements will differ. You may not share a design file or a breadboard.
Can we propose our own topic?	Encouraged. Bring a draft abstract by 12 August so there is time to iterate before the deadline.
Do we need to buy a multimeter?	No. The lab has them and most teams have access to one. If your team genuinely has none outside lab hours, tell us in Week 1 and we will arrange one.
How do we measure THD without a distortion analyser?	Capture the output with your laptop's sound card (properly attenuated) and take an FFT in Audacity, Visual Analyser or a ten-line Python script. Compute THD from the harmonic amplitudes. This is a real technique, not a workaround.
Our simulated and measured results differ by 20%. Is that bad?	That is normal for a breadboarded discrete analog circuit, and it is the most interesting part of your report. What would be bad is not explaining it. Differences above about 50% usually mean something is actually wrong — investigate rather than rationalise.
How long should the report be?	12–18 pages. A dense, well-argued 13 beats a padded 22. Calculations and raw data go in appendices.
Can we reuse a circuit from a textbook or a website?	You may start from a published topology — most topologies are standard. What must be yours is the design: every component value calculated by you for your specification, with the working shown. Cite the source of the topology.

18. Final Submission Checklist — 30 October 2026

Tick every line before submitting. Items marked ▣ are the ones most often missed.

- ☐ Abstract submitted on time (15 Aug), with a numerical specification, and any requested change made
- ☐ ▣ Design file complete — every component value has a calculation behind it, somewhere
- ☐ DC load line drawn, with designed and measured Q-points both marked
- ☐ ▣ SPICE files included, opening and running on another machine, with any custom model file
- ☐ ▣ Transistor model used is stated in the report, with its source
- ☐ Final schematic legible, all values and part numbers marked
- ☐ ▣ Raw measurement tables included, with the instrument and settings stated for each
- ☐ ▣ Measured β of the actual devices used, reported
- ☐ Photographs of the build: one overall, one close-up with legible wiring
- ☐ ▣ The three-way comparison table (designed / simulated / measured) is present and complete

☐ ▣ Every gap in that table is explained by a named mechanism, not by 'practical errors'

☐ Simulation-only teams: tolerance study and temperature sweep included

☐ ▣ Logbook submitted, with dated entries spanning August through October

☐ Troubleshooting section written, with at least one real episode

☐ All figures: axes labelled with units; frequency responses on log axes in dB; simulated and measured on shared axes

☐ Oscilloscope captures have volts/div and time/div stated in the caption

☐ Limitations section written honestly

☐ ▣ Appendix: contribution statement, signed by every member

☐ ▣ Appendix: AI tools declaration

☐ Minimum 6 references in IEEE style, including one course textbook and one datasheet

☐ Slides uploaded (max 15)

☐ ▣ Hardware brought to the demo, powered, with its own adapter and spare transistors

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Raise questions about scope, components or lab access early rather than late. Consultation slots are available during the tutorial hour each week; bring your logbook and your design file.

PCECT303 Analog Circuits — Course Project Handbook — Issued 06 August 2026